A Balanced Ka-Band GaAs FET MMIC Frequency Doubler

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Abstract— **A simplified and miniaturized state-of-the-art balanced GaAs FET MMIC frequency doubler operating at 36 GHz has been designed and realized in coplanar waveguide technology. The passive part of the circuit is designed using an effective, in-house developed quasi-static finite-difference method for the analysis of coplanar structures [1], [2] while the active device is characterized by using the Curtice-Ettenberg model [3]. The model makes use of the measured electrical values of the transistor and interpretes them through approximate empirical formulas. The results obtained demonstrate that by using simple models, which require very little computation time, it is possible to design an efficient frequency doubler in the Ka-band with a maximum conversion gain of 3 to 6 dB, without the need of using complicated transistor models or circuitry.**

I. Introduction

THE COPLANAR technology has attracted the attention of many MMIC designers in the recent years [4]–[7]. This is because it has the advantage of being truly planar and thus provides the possibility of on-wafer circuit tests, it permits easy connection of both series and shunt circuit elements, and it has low radiation losses in the odd mode. Moreover, CPW parameters are not sensitive functions of substrate thickness, and a wide range of impedance is achievable on reasonably thick substrates. These advantages can be assured only if a thorough investigation of the associated coplanar discontinuities such as T-junctions, bends, cross-junctions, and air-bridges is done and their effects are taken into account in the design. To characterize these discontinuities, accurate lumped element equivalent circuit models [1], [5] have been used. The balanced frequency doubler presented here is designed by taking the above mentioned effects into consideration. The discrepancy between simulation and measurement results obtained is within the limit of design tolerance.

II. Analysis and Design Method

In analyzing and designing a FET frequency doubler, the attention of the designer usually concentrates around the following two points:

1) The equivalent circuit model parameters of the FET must be determined from measurement values, something that cannot be done analytically.
2) The preconditions necessary for optimum doubler operation (such as dc bias, excitation level, and impedance matching) must be fulfilled.

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Regarding the first point, the parameters of the chosen transistor model (Curtice-Ettenberg model in our case) is determined and optimized by minimizing the discrepancy between the measured and simulated DC and RF quantities at every operating point. Regarding the second point, the following conditions can be used as a basis to set optimization criterea for doubler design:

1) One maximizes the ratio of the second-harmonic and the fundamental frequency power at the output, i.e $P_{\text{out}}(2\omega_0)/P_{\text{out}}(\omega_0)$, so that one obtains an output signal with maximum second harmonic distortion; or
2) one forms the ratio between the second harmonic power at the output and the fundamental power at the input, i.e $P_{\text{out}}(2\omega_0)/P_{\text{in}}(\omega_0)$, thereby maximizing or minimizing the resulting conversion gain or loss, respectively, as the case may be.

Regarding bias point, it has been theoretically and experimentally verified [8] that it is the variation of the gate-source voltage V_{gs} that has greater effect in causing nonlinear distortion, thus generating a waveform that is rich in second harmonic component. Assuming a constant value of V_{ds}, the drain current can be approximated as [3]:

$$i_{\text{ds}} = a_0' + a_1' v_{\text{gs}}^2 + a_2' v_{\text{gs}}^2 + a_3' v_{\text{gs}}^3, \tag{1}$$

where v_{gs} contains both the dc and ac voltage components of the input.

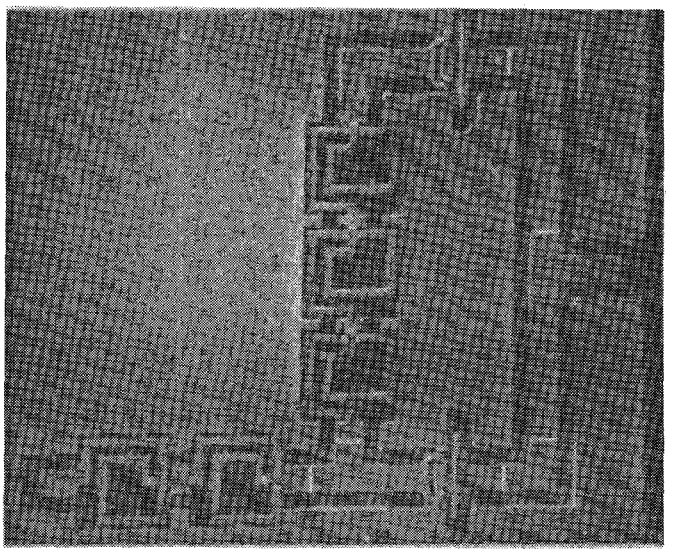
The coefficients a_0', a_1', a_2', a_3' are the Curtice-Ettenberg model parameters, where the effect of the tangent hyperbolic function in the model [3] has also been included.

Expressing v_{gs} as $v_{\text{gs}} = V_{\text{gs0}} + V_{\text{gs1}}\cos(\omega t)$, it can be shown that the optimum gate bias voltage V_{gs0}, necessary for optimum generation of the second harmonic is given by:

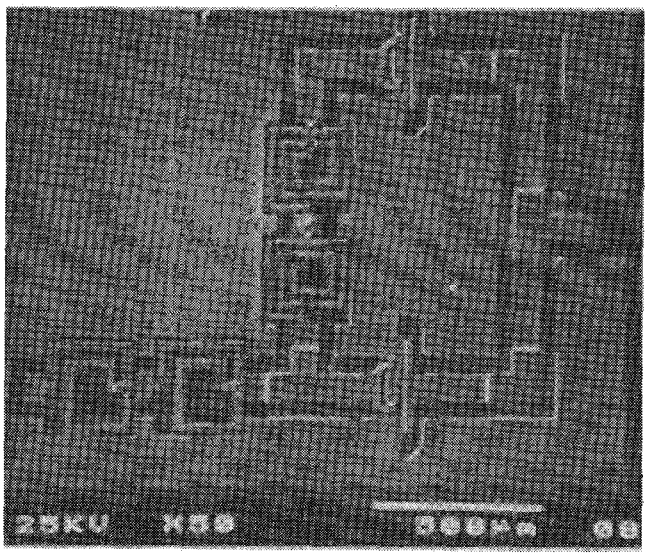
$$V_{\text{gs0}} = -\frac{1}{3}\left(\frac{a_2'}{a_3'}\right) + \sqrt{\frac{1}{4}V_{\text{gs1}}^2 + \frac{1}{3}\left(\frac{a_1'}{a_3'}\right) - \frac{1}{9}\left(\frac{a_2'}{a_3'}\right)^2} \tag{2}$$

This optimum voltage usually lies near pinch-off.

The balanced frequency doubler of the type proposed here basically consists of a pair of identical GaAs FET's, a 180° phase-shifting circuit designed using proper combination of spiral inductors, power splitter/combiner circuits, and impedance matching networks. The gates of the two transistors are driven by signals having a 180° phase difference, and this results in the mutual cancellation of the fundamental signals at the output while the second-harmonic signals combine and add up.



(a)



(b)

Fig. 1. (a) Photograph of the 36-GHz balanced MMIC frequency doubler, where three spiral inductors connected in series are used as the phase-shifting circuit. (b) Photograph of the 36-GHz balanced MMIC frequency doubler, where two spiral inductors connected in series are used as the phase-shifting circuit.

Fig. 1 shows the REM photograph of two versions of the realized balanced doubler. The first one ((Fig. 1(a)) utilizes three spiral inductors (of 1.5 turns each) connected in series for the purpose of phase shifting, and the second one ((Fig. 1(b)) uses only two spiral inductors, also connected in series, having 2.5 turns each. Simulation and measurement results showed that both doublers have identical performance. Obviously, the doubler with two spiral inductors has the advantage of being more compact (1.5 mm $\times$ 1.5 mm) and is, therefore, preferable for fabrication. On the other hand, the use of the 1.5-turn spiral inductor has the advantage of providing more capacitance to ground, which is usually necessary for impedance matching purposes. Moreover, its first resonant frequency is higher than the 2.5-turn inductor and, therefore, there is much less danger that this resonant frequency falls in the frequency range at which the circuit is desired to operate.

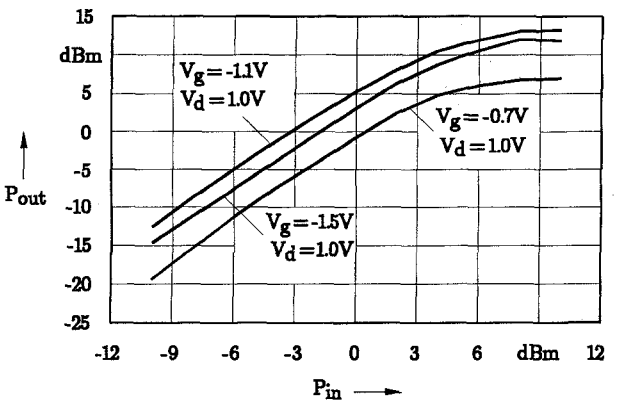


Fig. 2. Simulated second-harmonic output power as a function of the input power for different bias voltages of the transistor.

A new approach in coplanar technique is used for the design of the required impedance matching and phase-shifting circuits in that the parasitic capacitances of spiral inductors and the effects of the coplanar discontinuities have been fully exploited in the design. In this way, the conventionally used and space occupying 180° couplers, as well as the MIM capacitors, have been effectively eliminated. For the simulation, the coplanar line discontinuities and the spiral inductors are substituted by their lumped element equivalent circuits [5] and the transistors by the Curtice-Ettenberg nonlinear transistor model. The transistor type used for the design is a GaAs FET with 0.3 μm gate length and 200 μm gate width fabricated in coplanar technology at the Semiconductor Department of the University of Duisburg [9]. The overall circuit is simulated using a commercially available CAD harmonic balance simulator [10].

III. Results

To observe the effect of the bias voltage on the performance of the doubler, the output power is simulated for different operating point of the transistor. This is shown in Fig. 2, where the simulated dependence of the second-harmonic output power on the input power with the bias voltage taken as a parameter is drawn. The optimum operating gate voltage of the transistor is found to be -1.1 V. It is worth mentioning that, whereby the optimum bias point is sensitive to the variation of the gate voltage, it is not so to the variation of the drain voltage. To help compare the simulation results with the measurement results obtained, it makes sense to first re-simulate the circuit using the transistor parameters obtained from newly measured data of the transistor that is found on the wafer on which the whole doubler circuits is fabricated. The measured performance of the doubler is then compared with the newly simulated results. Fig. 3 shows the measured and the newly simulated output power of the doubler. The realized doubler has a conversion gain of 3 dB. This result is significant because doublers reported so far in this frequency range usually have conversion losses. Moreover, they do not take coplanar discontinuities into account and that makes our design approach unique. The doubler has a bandwidth of 3 to 4 GHz. However, the center frequency of the realized doublers has shifted by 2 to 3 GHz from the design value (36 GHz). This frequency shift can be

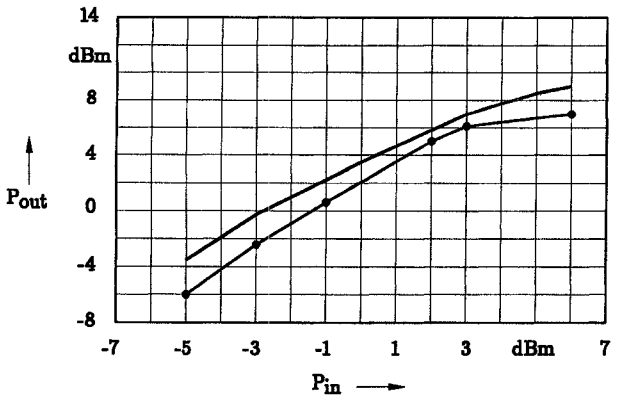


Fig. 3. Measured (dotted line) and simulated (solid line) output power of the 36-GHz balanced MMIC frequency doubler as a function of the input power.

attributed, among other things, to the technological difficulty in reproducing the transistor parameters accurately (after all the transistors used here are not industry products; they are, rather, fabricated at our university for research purposes). The fact that a simplified transistor model is used for the simulation also contributes to the discrepancy between measurement and calculation results. Nevertheless, the operating frequency lies within the design bandwidth of the circuit.

IV. Conclusion

A new CAD-based approach in the design of GaAs FET balanced frequency doubler has been applied in coplanar techniques. The design method exploits the parasitic effects of spiral inductors and coplanar line discontinuities in the design of the impedance-matching and phase-shifting circuits. A simplified transistor model has been used for the nonlinear simulation. Measurement results have verified the validity of the design approach used.

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